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In this paper we show how to exploit energy-delay trade-offs that exist due to the variation of the technology parameters for the implementation of interconnect wires. We also evaluate how these trade-offs can be propagated to the memory module level, so we can minimise the power consumption of the entire memory organisation (i.e., memories and connections between them). Our approach is that at future technology nodes the delay problem can be handled at the application level, so given any delay ...

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The proliferation of mobile and pervasive computing devices has brought energy constraints into the limelight. Energy-conscious design is important at all levels of system architecture, and the software has a key role to play in conserving battery energy on these devices. With the increasing popularity of spatial database applications, and their anticipated deployment on mobile devices (such as road atlases and GPS-based applications), it is critical to examine the energy implications of spatial ...

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David E. Lackey , Paul S. Zuchowski , Juergen Koehl
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Amit Sinha , Anantha P. Chandrakasan
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